IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

"APPLICANTS' BRIEF ON APPEAL IN ACCORDANCE WITH 37 CFR §41.37"

APPLICANT: Robert BAUMGARTNER et al.		GROUP ART UNIT: 2112
SERIAL NO.:	09/807,352	EXAMINER: Clifford H. KNOLL
FILING DATE:	June 28, 2001	CONFIRMATION NO.: 6267
INVENTION:	"DATA BUS AND METHOD FOR ESTABLISHING COMMUNICATION BETWEEN TWO MODULES BY MEANS OF SUCH A DATA BUS"	

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

This is an appeal, filed in the U.S. Patent and Trademark Office on June 9, 2005, of the Examiner's Final Rejection dated December 8, 2004, of claims 1 -12.

In accordance with 37 C.F.R. §41.37, this Brief is submitted with a check in the amount of $500.00 to cover the filing fee under §41.20(b)(2) and a request for a one month extension of the date for filing of the brief. Applicants hereby request a one month extension of the date for filing this brief to September 9, 2005, and enclose herewith a check in the amount of $120 for the fee.

The sections required under 37 C.F.R. §41.37(c)(1) are set forth below:

(i). REAL PARTY IN INTEREST

The real party in interest in the present appeal is the assignee, OCE Printing Systems GmbH, by recorded assignment as recorded on July 2, 2001, at Reel 011945, Frame 0761.

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(ii). RELATED APPEALS AND INTERFERENCES

No related appeals or interferences have been filed.

(iii). STATUS OF CLAIMS

Claims 1 - 12 are on appeal and are set forth as amended in the Claims Appendix attached hereto.

In the present application, claims 1 - 18 are pending.

Claims 1, 2, 4, 5, 11 and 12 are rejected in the Final Rejection under 35 U.S.C. 102(b) as being unpatentable over Lagoy U.S. Patent 4,918,645;

Claim 3 is rejected in the Final Rejection under 35 U.S.C. 103(a) as being unpatentable over Lagoy U.S. Patent 4,918,645 in view of Harrison U.S. Patent 5,337,411;

Claims 6 and 7 are rejected in the Final Rejection under 35 U.S.C. 103(a) as being unpatentable over the Lagoy U.S. Patent 4,918,645 in view of Alnuweiri U.S. Patent 5,572,687;

Claim 8 is rejected in the Final Rejection under 35 U.S.C. 103(a) as being unpatentable over the Lagoy U.S. Patent 4,918,645 in view of widely known design techniques as evidenced by Ammar (Understanding Advanced Bus-Interface Products); .

Claims 9 and 10 are rejected in the Final Rejection under 35 U.S.C. 103(a) as being unpatentable over the Lagoy U.S. Patent 4,918,645 in view of widely known design techniques as evidenced by Appelbaum U.S. Patent 5,758,188; and

Claims 13 - 18 are withdrawn from consideration.

(iv). STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Rejection.

(v). SUMMARY OF CLAIMED SUBJECT MATTER

Briefly, the present invention provides a parallel databus having a plurality of parallel signal lines to which a plurality of assemblies can be connected, whereby each assembly has a

databus driver being in immediate connection with the signal lines and has a controller that is connected to the databus driver. This databus is based on the known MULTIBUS II. The invention is characterized in that the databus drivers are connected to the clock generator of the databus, and that the databus drivers are fashioned such that the signals to be transmitted from and to the data and control lines are accepted during a clock pulse that is predetermined by the clock generator, and are emitted during the following clock pulse. As a result thereof, the signaling path between two assemblies connected via the databus is interrupted at the databus drivers, so that the signals cover a shorter path section during a clock pulse of the databus compared to conventional databuses with transparent databus drivers. The individual signal propagation times are thus reduced, so that the bus frequency of the databus and therefore the data throughput can be significantly increased.

The claims on appeal set forth the features of the present invention. With reference to the specification and drawings, Figure 2 and page 11, line 1 to page 12, line 20 of the substitute specification as presented in the Preliminary Amendment provide that the modules 8 to 10 represent assemblies 2 that are respectively connected to the databus 5, whereby each assembly has a databus driver 3 and a controller 4 (Figure 2). The databus 5 corresponds to the multibus II (multibus is a registered trademark of Intel Corp.), as it is defined in IEEE standard for "High Performance Synchronous 32-Bit Bus: MULTIBUS II The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, NY 10017, USA, 1998", apart from the changed cited in the following description.

The hardware realization of this databus 5 is composed of a backplane, in which the signal lines of the bus are arranged and which are provided with 20 to 25 cable connectors to which an assembly 2 can be respectively connected. The CSM module (Central Services Module), which executes specific start routines and which initializes the individual assemblies, represents such an assembly known from the multibus. The CSM module has a clock generator, which applies a clock signal oscillating with a predetermined bus frequency to a clock signal line of the databus 5. The bus frequency is 40 MHz in the present exemplary embodiment.

The databus drivers 3 of each assembly 2 are connected to the clock signal line 12, whereby the input and output of the databus drivers 3 can be clocked corresponding to the bus frequency or, respectively, the bus clock pulse.

In addition to the clock signal line 12, the databus 5 has further lines, such as 32 data lines for transmitting the data, control lines for controlling the data transmission, decision lines for deciding (arbitration), which assembly is allowed to access the databus 5, address lines and one or more lines for the supply voltage and ground. In the present exemplary embodiment, the same lines are used for transmitting the addresses and the data, so that combined address lines/data lines are present.

The databus drivers 3 are inventively connected to the clock signal line 12 and are fashioned such that the signals to be transmitted from and to the data lines and control lines are accepted during a clock pulse prescribed by a clock generator and are outputted during the following clock pulse. The part of the databus driver 3, which operates the data lines and control lines, therefore is fashioned as a non-transparent electronic component with a temporary storing function, as it can be realized by a D-flip-flop, for example. These databus drivers 3, during a clock pulse, therefore accept the signals of the data lines and control lines coming from the databus 5, they store them and output them to the respective controller 4 during the immediately following clock or, respectively, they accept a signal coming from the controller 4 during a clock pulse, they store said signal and apply it to the databus 5 at the immediately following clock pulse. The databus drivers 3 therefore are operated in a "clocked" fashion with respect to the data lines and control lines.

As shown in Figure 8 and 9 and described on page 21, lines 1 – 15, as it is known from the multibus, the control signals ARB (5. . 0) and a bus request signal BREQ (bus request) are used for the decision (arbitration). In contrast to the address signals/data signals and the control signals, these signals are not clocked-in, since the decision lines then cannot be used in a "wired-or-modus", which is used for deciding the access rights. The databus driver therefore is transparent for these signals. Since one clock pulse period is not sufficient as signal runtime from one controller to the other controller for transmitting the signals, the

databus is provided with an additional clock pulse signal line, whereby an auxiliary clock pulse BCLK2 is applied thereto. The auxiliary clock pulse BCLK2 (20 MHz) is generated by dividing the bus frequency by two.

The signals ARB (5 . . 0) and BREQ are generated by the assemblies in the high-phase of the auxiliary clock pulse and are also queried in the high-phase of the auxiliary clock pulse BCLK2. It is thus assured that at least two clock pulse periods of the bus frequency or, respectively, of the bus clock pulse are available to the signals as signal runtime.

As described on page 6, line 18, to page 7, line 2, the outputs of the databus driver leading to the controller may be fashioned as low- voltage TTL outputs. The signal lines preferably have a physical expanse of at least 40 cm. The signal lines may have a physical expanse of at least 50 cm. A plurality of the assemblies that are connected to the signal lines are respectively can be provided with a processor. The databus may be multibus-compatible.

(vi). GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) The first issue on appeal is whether Claims 1, 2, 4, 5, 11 and 12 are unpatentable under 35 U.S.C. §102(b) over Lagoy U.S. Patent 4,918,645;

2) The second issue on appeal is whether Claim 3 is unpatentable under 35 U.S.C. §103(a) over Lagoy U.S. Patent 4,918,645 in view of Harrison U.S. Patent 5,337,411;

3) The third issue on appeal is whether Claims 6 and 7 are unpatentable under 35 U.S.C. §103(a) over the Lagoy U.S. Patent 4,918,645 in view of Alnuweiri U.S. Patent 5,572,687;

4) The fourth issue on appeal is whether Claim 8 is unpatentable under 35 U.S.C. §103(a) over the Lagoy U.S. Patent 4,918,645 in view of widely known design techniques as evidenced by Ammar (Understanding Advanced Bus-Interface Products); and

5) The fifth issue on appeal is whether Claims 9 and 10 are unpatentable under 35 U.S.C. §103(a) over the Lagoy U.S. Patent 4,918,645 in view of widely known design techniques as evidenced by Appelbaum U.S. Patent 5,758,188.

(vii). ARGUMENT

With respect to each ground of rejection identified for review in section (vi), the following arguments are presented.

1) Claims 1, 2, 4, 5, 11 and 12 are not anticipated under 35 U.S.C. §102(b) over the Lagoy U.S. Patent 4,918,645.

The Lagoy reference discloses a page mode type of memory access. A requesting agent requests data from a replying agent over a system bus. The request initiates an access cycle to access the memory by strobing the row and column signals according to a pattern to obtain pages of data.

With respect to claim 1, the claim includes as one element a databus driver that is a non-transparent electronic device. The specification of the present invention explains that prior databus drivers are transparent electronic physical units, i.e., the respective corresponding input side and output side of the databus driver assumes the same logical value.

In the final rejection, the Examiner takes the position that the Lagoy reference discloses a non-transparent databus driver and controller. The Lagoy reference has been reviewed by the inventor, who concludes that the reference does not show a non-transparent databus driver and controller. In particular, Lagoy shows in Fig. 5 the data latch 72 which is connected to the signal line 66j for the signal DEN0. The data latch is connected to the system bus 10 and to the memory databus 74. To read and write data from and to the systembus 10, the data latch needs an enable signal. This enable signal is the signal DEN0. In column 7, line 60, of the reference the signal DEN0 is described as to enable the above data latch 72 for placing the data from the memory data bus 74 onto the system bus 10. Thus, no clock-signal is provided to the data latch 72.

The Examiner takes the position that the CAS signal is a clock signal, but the signal diagram in the reference shows that it is not a clock signal, but a signal to permit paging of the data with patterns of 0s and 1s to accomplish the page mode data transfer.

Furthermore, according to the Examiner's point of view the broadest reasonable interpretation of the term "non-transparent" is based on the assertion that the term is met by a buffer that is double-clocked, in other words a buffer that clocks data in and subsequently clocks data out.

Firstly, the latch 72 is not clocked. Thus, the buffer 72 of Lagoy is not covered by the interpretation of "non-transparent" of the Examiner.

Secondly, the Examiner's interpretation is not correct, as "transparent" means in connection with a buffer that the same signals as are applied to the input side are always available as well as at the output side. A "non-transparent" buffer is a buffer being clocked in such a way that during a clock pulse different signals are applied to the input side and to the output side of the buffer. Such a "non-transparent" buffer cannot be used in the prior art according to Lagoy, as no clock signal is directed to the latch 72.

In this respect Applicant points out that according to the invention as shown in Fig. 4, different data words are simultaneously transmitted from the transmitter assembly S to the databus driver and from the databus driver of the transmitter assembly S to the data bus driver of the receiver assembly. This is obviously only possible, when the data bus driver is fashioned as a non-transparent electronic component.

Thus, the present invention as defined in claim 1 is not anticipated by the Lagoy reference.

Claims 2, 4, 5, 11 and 12 are not argued separately.

2) Claim 3 is not obvious under 35 U.S.C. §103(a) over Lagoy U.S. Patent 4,918,645 in view of Harrison U.S. Patent 5,337,411.

The Lagoy reference teaches an apparatus that lacks a clock signal connected to the latch, so that it is not possible to simultaneously transmit different data words from the transmitter assembly to the databus driver and from the databus driver to the transmitter assembly. In view of the differences in operation, it would not be obvious to modify the Lagoy reference to provide the non-transparent driver as claimed.

The Harrison reference discloses a multi-drop bus architecture with up to 16 processors. Higher bus clock frequencies are taught. The characteristics of the present databus driver is not suggested, however. As such, the claimed invention as defined in claim 3 is not obvious over even the combination.

3) Claims 6 and 7 are not obvious under 35 U.S.C. §103(a) over the Lagoy U.S. Patent 4,918,645 in view of Alnuweiri U.S. Patent 5,572,687.

The comments concerning the Lagoy reference are set forth above and are referenced here without being repeated.

The Alnuweiri reference discloses a bus apparatus and synchronous priority arbitration between modules. With respect to claim 6, the Alnuweiri reference discloses an arbitration process using a four line arbitration bus. Mention is made of the timing signals of the arbitration lines in the passage cited by the Examiner (col. 9, lines 59 – 64). However, Applicants find no teaching of a device for generating an auxiliary clock pulse with a lower frequency than the bus frequency. Absent such teaching, the combination of Lagoy and Alnuweiri do not obviate the invention as claimed.

With respect to claim 7, Applicant submits that a frequency divider connected and operating as claimed is not shown in the Alnueiri reference. As such, even when considered together with Lagoy, the claimed invention is not shown or suggested.

4) Claim 8 is not obvious under 35 U.S.C. §103(a) over the Lagoy U.S. Patent 4,918,645 in view of widely known design techniques as evidenced by Ammar (Understanding Advanced Bus-Interface Products).

The comments concerning the Lagoy reference are set forth above and are referenced here without being repeated.

The Ammar reference is cited only for the showing of low voltage TTL drivers. This reference in combination with Lagoy does not suggest the claimed combination.

5) Claims 9 and 10 are not obvious under 35 U.S.C. §103(a) over the Lagoy U.S. Patent 4,918,645 in view of widely known design techniques as evidenced by Appelbaum U.S. Patent 5,758,188.

The comments concerning the Lagoy reference are set forth above and are referenced here without being repeated.

With respect to claim 9, Appelbaum is merely cited for its showing of known bus lengths. Appelbaum with Lagoy does not suggest the inventive databus drivers.

Claim 10 is not separately argued.

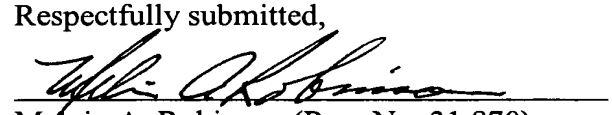
Thus, each of the §103 rejections has been shown to be unsupported by the art. As such, the claimed invention is a non-obvious improvement over the teachings of the prior art references, alone or in combination. Favorable reconsideration of the claims is hereby requested.

CONCLUSION

Applicants submit that the subject matter of the claims 1-12 on appeal is not found in any of the references cited by the Examiner, taken singly or in combination, and those claims are therefore allowable.

Applicants respectfully submit that the Examiner is in error in law and fact in rejecting the claims 1 – 12 and earnestly solicit reversal of the Final Rejection and allowance of all claims.

Respectfully submitted,



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(viii). CLAIMS APPENDIX

A copy of the claims involved in the appeal is set forth below:

1. A parallel databus assembly, comprising:

a plurality of parallel signal lines;

a plurality of assemblies connected to said plurality of parallel signal lines, each of said assemblies having

a databus driver being in immediate connection with said signal lines, and

a controller connected to said databus driver,

at least some of said plurality of parallel signal lines being at least one of data lines for transmitting data and control lines for controlling data transmission of the data via said data lines,

a clock generator generating a predetermined bus frequency with which signals transmitted in said signal lines are clocked,

said databus drivers being connected to said clock generator, said databus drivers being fashioned such that signals to be transmitted over said data lines and said control lines are accepted during a clock pulse prescribed by said clock generator and are emitted during a further clock pulse following said clock pulse, said databus driver being a non-transparent electronic device.

2. A parallel databus assembly according to claim 1, wherein said clock generator generates a bus frequency of at least 20 MHz.

3. A parallel databus assembly according to claim 2, wherein said clock generator generates a bus frequency of approximately 40 MHz

4. A parallel databus assembly according to claim 1, wherein said databus has 32 data lines.

5. A parallel databus assembly according to claim 1, wherein further ones of said plurality of parallel signal lines are fashioned as decision lines for deciding which of said plurality of assemblies connected to said parallel signal lines has access priority, and

said databus drivers having non-clocked open-drain outputs connected to said decision lines a wired-or logic is formed.

6. A parallel databus assembly according to claim 5, further comprising:

a device for generating an auxiliary clock pulse with a lower frequency than the bus frequency is provided for driving the decision lines.

7. A parallel databus assembly according to claim 6, wherein said device for generating an auxiliary clock pulse is a frequency divider.

8. A parallel databus assembly according to claim 1, wherein outputs of the databus driver leading to the controller are fashioned as low- voltage TTL outputs.

9. A parallel databus assembly according to claim 1, wherein said signal lines have a physical expanse of at least 40 cm.

10. A parallel databus assembly according to claim 1, wherein said signal lines have a physical expanse of at least 50 cm.

11. A parallel databus assembly according to claim 1, further comprising:

a processor for a plurality of the assemblies that are connected to the signal lines .

12. A parallel databus assembly according to claim 1, wherein said databus is multibus-compatible.

Claims 13 – 18 have been withdrawn from consideration and are not on appeal.

(ix). EVIDENCE APPENDIX

No further evidence is being submitted.

(x). RELATED PROCEEDINGS APPENDIX

There are no relate proceedings.

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